UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,275	04/08/2004	Jeffery W. Janzen	501286.01 (30262/US)	2177

27076 7590 02/12/2009

DORSEY & WHITNEY LLP
INTELLECTUAL PROPERTY DEPARTMENT
SUITE 3400
1420 FIFTH AVENUE
SEATTLE, WA 98101

EXAMINER	
ELAND, SHAWN	
ART UNIT	PAPER NUMBER
2188	

MAIL DATE	DELIVERY MODE
02/12/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/822,275	JANZEN, JEFFERY W.	
	Examiner	Art Unit	
	SHAWN ELAND	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/15/08 & 10/08/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-30 are pending in the Application.

Claims 1, 10, 21 and 26 are amended.

Claims 1-30 are rejected.

Response to Amendment

Applicant's amendments and arguments filed on 10/30/08 in response to the office action mailed on 06/16/08 have been fully considered, but they are moot in view of the new grounds of rejections.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 8 and 19 recite the limitation "the data bus" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim, as a plurality of data busses are previously set forth in these claims (i.e. each memory device includes a data bus). Which bus is being referenced by the phrase "the bus" in these claims?

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-30 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 42 of copending Application No. 11/417,389 (hereinafter Application '379) in view of ***Ryan*** (US PG Publication 2004/0044833 A1), and in further view of ***Schumacher*** (US Patent 5,502,621). The minor differences between claim 21 (selected as representative of the remaining base claims of the instant application as it is the most comprehensive of the set) of the instant application and claim 37 of the co-pending application are presented in the matrix below.

Instant Application 10/822,275	Co-pending Application 11/417,389
Claim 21:	Claim 42:
A computer system, comprising: a data input device;	A memory module, comprising:
a data output device;	
a processor coupled to the data input and data output devices;	
a controller electrically coupled to the processor, the controller being operable to receive and transmit memory signals on a high-speed data link;	
at lease one memory module coupled to the controller, each memory module comprising:	
a circuit board;	a circuit board;
a memory hub positioned on the circuit board;	a memory controller positioned on the circuit board;
a plurality of pairs of memory devices positioned around the memory hub and arranged in pairs on the same side of the circuit board as one another,	a plurality of memory devices positioned around the memory hub and arranged in pairs,
each memory device having the same physical layout including pins associated with a first functional group of signals adjacent a first end of each memory device and pins associated with a second functional group of signals adjacent a second end of each memory device, and the first end of each device in each pair being positioned substantially abutting one another on the circuit board;	each memory device having a first edge and a second opposite the first edge and further having a same arrangement of electrical terminals relative to the first and second edges, including a first group of electrical terminals to which first-type signals are coupled and a second group of electrical terminals to which second-type signals are coupled, the first group of electrical terminals positioned adjacent the first edge and the second group of electrical terminals positioned adjacent the second edge, the second edge of each device in a pair positioned adjacent a second edge of a memory device in one of the other pairs
a plurality of command-address busses, each command-address bus coupled to a port on the memory hub and at least one of the pins associated with the second functional group of signals on each of the at least two memory devices, the two memory devices being from a different pair; and	a plurality of command-address busses, each command-address bus electrically coupled to the memory hub and to a memory device of at least two pairs of memory devices, the command-address bus having the same length, wherein the command-address buses are diagonally routed with respect to an edge of the memory hub;

and an *edge* connector *positioned along an edge of the circuit board* and coupled to the memory hub.	a connector coupled to the memory hub and configured to couple at least one of command, address, and data signals to the memory hub

Note Ryan teaches several of the elements that claim 42 of Application '379 lacks, including:

a data input device (Fig. 3 (311));

a data output device (Fig. 3 (312));

a processor coupled to the data input and data output devices (Fig. 3 (304));

a controller electrically coupled to the processor, the controller being operable to receive and transmit memory signals on a high-speed data link (paragraph 0019, all lines);

a memory hub positioned on the circuit board (Fig. 3 element 208);

memory devices on the same side of a circuit board (again, Fig. 3); and

an edge connector positioned along the edge of the circuit board (memory modules are described as being DIMM devices – paragraph 0006, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Application '379 to further include Ryan's system and method for optimizing interconnections of memory devices in a multichip module into his own system for mirroring memory devices. By doing so, Application '379 would be able to exploit the timing benefits of Ryan's system including minimizing skew, and maximizing signal integrity between the hub and memory devices by positioning them equidistant from a centralized hub as taught by Ryan in paragraphs 0012 through 0013, all lines.

Despite these teachings Ryan fails to teach each memory device being positioned in a pairs, in which the paired devices are arranged such that each respective device has the same pinout, yet one is rotated 180 degrees with respect to the board such that first and second sets of functional pins are substantially abutting each other.

Schumacher however teaches arranging ICs in a paired configuration such that one device is rotated 180 degrees with respect to the board – Fig. 4, devices 410 and 415 are ICs with the same pinout, just mirrored with respect to the vertical axis (i.e. 180 degree rotation). Schumacher teaches this configuration (i.e. chips substantially abutting one another) in order to keep similar functional pin groupings together (col. 3, lines 40-56).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Application '379 to further include Schumacher's system of mirrored pin assignment for two sided multi-chip layout into his own system for mirroring memory devices. By doing so, Application '379 would be able to connect the memory devices of the memory system with a more simplified lead routing scheme, which in turn would lead to a reduction of the number of layers in the PCB as taught by Schumacher in col. 2 lines 35-39.

The remaining claims 1-20 and 22-30 are further rejected as being obvious over claim 42 of Application '379 in further view of ***Ryan*** (US PG Publication 2004/0044833 A1) in further view of ***Schumacher*** (US Patent 5,502,621). The minor differences between the copending claims and the pending claims of the instant application are rendered obvious in view of the combined teachings of Ryan and Schumacher based on the rationale set forth under the art rejections of these claims as discussed supra.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Response to Arguments

As for claims 8 and 19 (with respect to the § 112(2) rejections), Applicant failed to address the previous rejections either in argument or by way of amendment; therefore these rejections are maintained and restated above.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SHAWN ELAND whose telephone number is (571)270-1029. The examiner can normally be reached on Monday - Friday, 8 - 4 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on (571)272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hyung S. Sough/
Supervisory Patent Examiner, Art Unit 2188
02/02/09

/ SHAWN ELAND /
Examiner, Art Unit 2188